WHAT IS CLAIMED IS:

1. A microprocessor, comprising:

an instruction cache;

a trace cache; and

a prefetch unit coupled to the instruction cache and the trace cache;

wherein the prefetch unit is configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache.

2. The microprocessor of claim 1, wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions that correspond to operations that precede a branch in the evicted trace.

3. The microprocessor of claim 1, wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions that correspond to operations that follow a branch in the evicted trace.

4. The microprocessor of claim 1, wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache.

5. The microprocessor of claim 4, wherein the prefetch unit is configured to fetch a number of lines that is proportional to the number of branch operations comprised in the evicted trace.

6. The microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the

eviction of certain traces from trace cache if the line of instructions is already stored in instruction cache.

7. The microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the eviction of certain traces from trace cache if the evicted trace is predicted unlikely to re-execute.

8. A computer system, comprising:

a system memory; and

a microprocessor coupled to the system memory, comprising:

an instruction cache;

a trace cache; and

a prefetch unit coupled to the instruction cache and the trace cache;

wherein the prefetch unit is configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache.

9. The computer system of claim 8, wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions which correspond to operations that precede a branch in the evicted trace.

10. The computer system of claim 8, wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions which correspond to operations that follow a branch in the evicted trace.

11. The computer system of claim 8, wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache.

12. The computer system of claim 11, wherein the prefetch unit is configured to fetch a number of lines that is proportional to the number of branch operations comprised in the evicted trace.

13. The computer system of claim 8, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the eviction of certain traces from trace cache if the line of instructions is already stored in instruction cache.

14. The computer system of claim 8, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the eviction of certain traces from trace cache if the evicted trace is predicted unlikely to re-execute.

15. A method, comprising:

evicting a trace from a trace cache;

fetching a line of instructions into an instruction cache in response to said evicting.

16. The method of claim 15, further comprising checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace.

17. The method of claim 16, further comprising inhibiting the fetching of the line of instructions into the instruction cache if the line of instructions is stored in the instruction cache.

18. The method of claim 15, further comprising predicting the likelihood that the evicted trace will be re-executed and inhibiting said fetching of the line of instructions into the instruction cache if the evicted trace is predicted unlikely to re-execute.

19. The method of claim 15, wherein said fetching comprises fetching a line from instruction cache comprising instructions that correspond to operations that precede a branch in the evicted trace.

20. The method of claim 15, wherein said fetching comprises fetching a line from instruction cache comprising instructions that correspond to operations that follow a branch in the evicted trace.

21. The microprocessor of claim 15, wherein said fetching comprises fetching a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache.

22. The microprocessor of claim 15, wherein the number of lines fetched is proportional to the number of branch operations comprised in the evicted trace.

23. A microprocessor comprising:

means for evicting a trace from trace cache;

means for fetching one or more lines into instruction cache in response to said evicting.